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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/637,166	08/08/2003	Marc Tremblay	SUN-P9323-SPL	2934

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EXAMINER

JOHNSON, BRIAN P

ART UNIT PAPER NUMBER

2183

DATE MAILED: 01/30/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/637,166	Applicant(s) TREMBLAY ET AL.	
	Examiner Brian P. Johnson	Art Unit 2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 08 August 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

1. Claims 1-20 have been examined.

Acknowledgment of papers filed: oath, specification, drawings, and IDS, on August 8th, 2003. The papers filed have been placed on record.

Specification

2. The title is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-5, 10-11, 13, and 18-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Rajwar (Speculative Lock Elision by Ravi Rajwar and James R. Goodman).

5. Regarding claim 1 and 13, Rajwar discloses a method for executing a start transactional execution (STE) instruction (page 297 col 1 lines 23-25)

Note that the reference discloses the use of a "critical section". The first instruction within that critical section is considered to be the "start transactional execution instruction".

To facilitate transactional execution on a processor (page 297 col 1 lines 13-15), comprising: encountering the STE instruction during execution of a program, wherein the STE instruction marks the beginning of a block of instructions to be executed transactionally (see below);

Note that, as explained above, the STE instruction of the reference is considered to begin the block of instructions to be executed transactionally (critical section).

And upon encountering the STE instruction, commencing transactional execution of the block of instructions following the STE instruction (page 297 col 1 lines 23-25); wherein changes made during the transactional execution are not committed to the architectural state of the processor until the transactional execution successfully completes (page 299 section 5.2 part 2).

6. Regarding claims 2 and 14, Rajwar discloses the method and apparatus of claims 1 and 13, wherein the STE instruction specifies an action to take if transactional execution of the block of instructions fails.

7. Regarding claims 3 and 15, Rajwar discloses the method and apparatus of claims 2 and 13, wherein the action to take can include branching to a location specified by the STE instruction.

8. Regarding claims 4 and 16, Rajwar discloses the method and apparatus of claims 2 and 14, wherein the action to take can include acquiring a lock on the block of instructions.

9. Regarding claims 5 and 17, Rajwar discloses the method and apparatus of claims 2 and 13, wherein the action to take can include setting state information within the processor to indicate a failure during transactional execution of the block of instructions, thereby enabling other software executed by the processor to manage the failure.

10. Regarding claims 6 and 18, Rajwar discloses the methods of claims 1 and 13, wherein if the transactional execution completes without encountering an interfering data access from another process or other type of failure, the method further comprises: atomically committing changes made during the transactional execution, and resuming normal non-transactional execution (page 298 col 1 part 5).

11. Regarding claim 7 and 19, Rajwar discloses the method and apparatus of claims 1 and 13, wherein if an interfering data access from another process is encountered during the transactional execution, the method further comprises: discarding changes made during the transactional execution; and attempting to re-execute the block of instructions (page 298 col 1 part 4).

12. Regarding claims 8 and 20, Rajwar discloses the method and apparatus of claims 1 and 13, wherein potentially interfering data accesses from other processes are allowed to proceed during the transactional execution of the block of instructions (page 297 col 1 lines 23-25).

13. Regarding claim 9, Rajwar discloses the method of claim 1, wherein the block of instructions to be executed transactionally comprises a critical section (page 297 col 1 lines 23-25).

14. Regarding claim 10, Rajwar discloses the method of claim 1, wherein commencing transactional execution of the block of instructions involves: saving the state of processor registers (page 299 sect 5.2 par 4-5); configuring the processor to mark cache lines during loads that take place during transactional execution; configuring the processor to mark cache lines during stores that take place during transactional execution (page 296 sect 2.2 first paragraph); and configuring the processor to continually monitor data references from other threads to detect interfering data references (page 298 col 1 part 4).

Note that the term "if hardware cannot provide atomicity" clearly implies that interferences are monitored.

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15. Regarding claim 11, Rajwar discloses the method of claim 1, wherein the STE instruction is a native machine code instruction of the processor (see below).

Note that, considering that an STE instruction (within the reference) is considered to be the first instruction in a critical section, it must be a processor-readable instruction, making it a "native machine code instruction of the processor".

Claim Rejections - 35 USC § 103

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

17. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Rajwar in view of common art.

18. Regarding claim 12, Rajwar discloses the method of claim 1, wherein the STE instruction is defined in a platform-independent programming language (see below).

Note that Examiner asserts that it is common practice to use platform-independent languages that are later assembled into native machine code, in this case causing the STE instruction to be defined in a platform-independent programming language.

Rajwar, at the time of the invention, would have been clearly motivated to use platform-independent programming language. "High level" languages, as they are called, are cheaper and easier to create and have been commonly used in the art for many years.

It would have been obvious at the time of the invention to use a platform-independent programming language for the STE instruction within the processor of Rajwar.

19. Claims 2-5 and 14-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rajwar in view of Enhancing Software Reliability with Speculative Threads (herein Lam).

20. Regarding claims 2 and 14, Rajwar discloses the method and apparatus of claims 1 and 13.

Rajwar fails to disclose the STE instruction specifying an action to take of transactional execution of the block fails.

Lam discloses a TRY instruction that indicates a checkpoint that is used in case of an interruption in a transactional section (section 3.2 col 2 TRY instruction).

Although it is clear from Rajwar that interruptions are restored, it does not give a specific description of how this is done. Lam, however, uses this TRY instruction which "allows the program to recover from attacks that overwrite data structures beyond those expected". Rajwar would be further motivated to use this technique because it gives a

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large amount of control to the programmer, who can remove unnecessary processor commands (which happened to be the general motivation behind the Rajwar invention initially).

It would have been obvious at the time of the invention for one of ordinary skill in the art to allow the STE instruction of Rajwar, the first instruction within a block of executed data, to give an explicit command including a "savepoint" command (as disclosed in Lam) or other recovery information as disclosed in Rajwar to the processor. This "savepoint" is considered to be a specific action to take if a transactional execution of the block fails.

21. Regarding claims 3 and 15, Rajwar/Lam discloses the method and apparatus of claims 2 and 14, wherein the action to take can include branching to a location specified by the STE instruction (see below).

Note that the STE instruction, as combined above, contains a savepoint that will update the program counter to a point different than normal program flow, interpreted by Examiner to be "branching to a location specified by the STE instruction".

22. Regarding claims 4 and 16, Rajwar/Nainani discloses the method and apparatus of claims 2 and 14, wherein the action to take can include acquiring a lock on the block of instructions (page 295 col 1 3rd paragraph lines 12-13).

23. Regarding claimd 5 and 16, Rajwar/Nainani discloses the method and apparatus of claims 2 and 14, wherein the action to take can include setting state information within the processor to indicate failure during transactional execution of the block of instructions (page 299 section 5.2 part 2 and section 3.2), thereby enabling other software executed by the processor to manage the failure (see below).

Note that the re-executed software code is part of the mechanism that manages the failure.

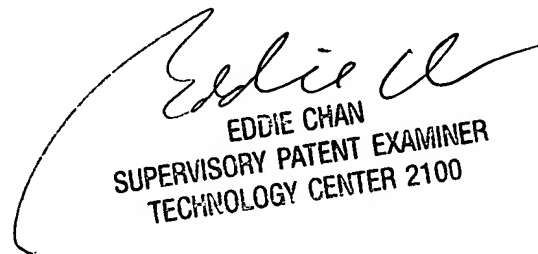
Conclusion

24. The following is text cited from 37 CFR 1.11(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian P. Johnson whose telephone number is (571) 272-2678. The examiner can normally be reached on 8-4:30 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



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